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Presented for filing is a new continuation patent application of:

Applicant: HISASHI OHTANI

Title: METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

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The prior application is assigned of record to Semiconductor Energy Laboratory Co., Ltd., a Japanese corporation, by virtue of an assignment recorded in the Patent and Trademark Office on February 19, 1998 at Reel/Frame 9012/0254.

Enclosed are the following papers, including those required to receive a filing date under 37 CFR 1.53(b):

	Pages
Specification	15
Claims	3
Abstract	1
Declaration	3 (from parent case)
Drawing(s)	6

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Enclosures:

- — Rule 63 declaration, copy from a previous application under rule 63(d) for continuation or divisional only.
- — Information Disclosure Statement: Applicant calls attention to documents listed on attached form PTO-892 (2 pages) from parent case. Per Rule 97(d) copies of those documents are not provided.
- — Postcard.

This application is a continuation (and claims the benefit of priority under 35 USC 120) of U.S. application serial no. 09/026,888, filed February 19, 1998. The disclosure of the prior application is considered part of (and is incorporated by reference in) the disclosure of this application.

Priority under 35 USC §119 is claimed based on Japanese application no. 9-53843, filed February 20, 1997.

Preliminary Amendment:

Page 1 of the specification, before line 1, insert—This is a continuation of U.S. application serial no. 09/026,888, filed February 19, 1998.

7 Total Claims; 3 Independent.

Basic filing fee	$690
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Independent claims in excess of 3 times $78	$0
Fee for multiple dependent claims	$0
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APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

APPLICANT: HISASHI OHTANI

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METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of manufacturing a semiconductor device using semiconductor with crystallinity.

2. Description of the Related Art

There has been known a thin film transistor (hereinafter referred to as "TFT") using thin film semiconductor. The TFT is made up of thin film semiconductor formed on a substrate. The TFT is used in a variety of integrated circuits, and in particular, attention is paid to the TFT as a switching device disposed in each pixel and a driver device formed on a peripheral circuit section in an active matrix-type liquid-crystal display device.

Up to now, an amorphous silicon film has been employed as a thin film semiconductor for use in a TFT, but in order to obtain higher performance, an attempt has been made to use a silicon film (crystalline silicon film) having crystallinity.

The TFT using the crystalline silicon film enables higher speed operation than that using the amorphous silicon film by two digits or more, and enables the manufacturing peripheral drive circuit of the liquid crystal display device which has been formed of an external IC, on a substrate on which an active matrix circuit is also formed.

The conventional crystalline silicon film is obtained by crystallizing an amorphous silicon film formed through a plasma CVD method or a low pressure CVD method, by a heat treatment or the irradiation of a laser light.

However, the method of crystallizing the amorphous silicon film by heating suffers from the following problems although it has an advantage that the crystalline silicon thin film can be obtained over a large area.

(1) A high heating temperature is required (it is difficult to use a glass substrate).

(2) The obtainable crystallinity is insufficient.

On the other hand, the method of crystallizing the amorphous silicon film by the

irradiation of a laser light suffers from a problem that high productivity and large-area processing are difficult although it has superiority that a glass substrate can be used as the substrate.

Under the above-described circumstances, the present inventors have developed a technique in which metal elements that promote the crystallization such as nickel, palladium, lead or the like are added to the amorphous silicon film to obtain the crystalline silicon film through a heat treatment conducted at a lower temperature than the conventional one (refer to Japanese Patent Unexamined Publication No. Hei 7-130652).

This method not only enables a crystallizing rate to increase so that crystallization can be achieved in a short time, but also enables high crystallinity to be uniformly obtained over a large area in comparison with the conventional method of crystallizing the amorphous silicon film by only heating or the crystallization of the amorphous silicon film by means of only the irradiation of a laser light.

The above-described crystallizing method using the metal elements will be roughly described hereinafter. First, as shown in Fig. 5A, a silicon oxide film 502 is formed on a glass substrate 501 as an under film, and an amorphous silicon film 503 is then formed on the silicon oxide film 502.

Subsequently, UV rays are applied to the amorphous silicon film 503 in an oxygen atmosphere to form an extremely thin oxide film on a surface of the amorphous silicon film. This is for preventing a solution containing nickel which will be introduced therein later from being repelled by the surface of the amorphous silicon film.

Thereafter, a mask 504 made of the silicon oxide film is formed. Then, an opening 505 is then defined in the mask 504. Further, a solution containing nickel therein is coated on the surface, and a excessive solution is blown off by a spin coater, to thereby obtain a state where a small amount of solution is held as indicated by reference numeral 506 (Fig. 5B).

Sequentially, a heat treatment is conducted to make crystal growth in parallel with a substrate indicated by reference numeral 508.

In this process, the growth is hindered by the mask 504 made of the silicon oxide film.

It is presumed that this is caused by a stress exerted between the mask 504 and the silicon film, but its details are not clear.

In order to prevent this problem, it is proposed that after the state shown in Fig. 5B, the mask 504 is removed to conduct a heat treatment. However, in this case, nickel is also removed together, which will adversely affect crystallization to be conducted later.

SUMMARY OF THE INVENTION

The present invention has been made in order to solve the above-described problems, and therefore an object of the present invention is to provide a technique of removing hindrance to crystal growth made in parallel to the above-described substrate.

In order to achieve the above-described object, according to one aspect of the present invention, there is provided a method of manufacturing a semiconductor device, comprising the steps of:

removing a part of an amorphous silicon film formed on a substrate having an insulating surface to form a region for introducing metal elements that promote crystallization of silicon;

allowing the region for adding said metal elements to selectively hold said metal elements; and

conducting a heat treatment to allow crystal growth from said metal element added region toward a direction in parallel to the substrate.

Also, in the above method, the introduction of said metal elements is conducted by coating a solution containing metal elements therein, and the selective holding of said metal elements is conducted by using water repellency of the silicon film to said solution.

Further, in the above method, in crystal growth, a surface of a region where crystal growth is conducted is exposed.

Also, according to another aspect of the present invention, there is provided a method of introducing metal elements that promote the crystallization of silicon from a surface of an amorphous silicon film, comprising the step of:

selectively controlling hydrophobic property of the surface of the amorphous silicon film to positionally control an introduced amount of said metal elements.

In this method, with positional control of the hydrophobic property of the surface of the amorphous silicon film, the metal elements are selectively introduced.

For example, an oxide film is formed on a part of the amorphous silicon film with the result that the wettability of that region is improved. Then, the solution containing the metal elements therein is coated on the surface in that state so that the metal elements can be introduced in only that region, or an introduced amount of the metal elements can be increased only in that region.

The most preferable metal elements that promote the crystallization of silicon is Ni from the viewpoint of the effect and reproducibility.

Also, the metal elements to be used may be one or plural kinds of elements selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

As a starting film, an amorphous film which is made of a silicon compound may be used instead of the amorphous silicon film. For example, an amorphous film indicated by Si_xGe_{1-x} ($0<x<1$) may be used.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1C are cross-sectional views each showing the vicinity of an opening into which metal elements are added at the time of crystallization according to the present invention;

Figs. 2A to 2D are diagrams showing a process of manufacturing a thin film transistor of the first embodiment;

Figs. 3E to 3H are diagrams showing a process of manufacturing a thin film transistor of the first embodiment;

Figs. 4I to 4K are diagrams showing a process of manufacturing a thin film transistor of the first embodiment;

Figs. 5A to 5C are diagrams showing a crystallizing method in a conventional example; and

Fig. 6A to 6F are diagrams showing a process of manufacturing a thin film transistor of the second embodiment.

DETAILED DESCRIPTION OF THE EMBODIMENTS

First, an amorphous silicon film 203 is formed (Fig. 2A).

Then, a part of the amorphous silicon film 203 is removed to form a region into which metal elements indicated by reference numeral 205 are introduced (Fig. 2B).

Subsequently, a solution (for example, nickel acetate solution) containing nickel elements therein which exhibits a water repellency (hydrophobic property) is coated on an entire surface of the amorphous silicon film 203.

Generally speaking, the amount of the metal elements contained in the solution is desirably set so as to be 1 ppm to 200 ppm, preferably 1 ppm to 50 ppm (weight conversion) with respect to the solution when the metal elements are nickel, although it depends on the kind of solution. This is a value determined in view of the concentration of nickel and a hydrofluoric acid resistivity in the film after the completion of crystallization.

In a state shown in Fig. 2B, the solution as coated is repelled by the surface of the amorphous silicon film.

As a result, the solution exists in only the region where a part of the amorphous silicon film has been removed (in this region, an under film 202 is exposed), as shown in Fig. 2C.

In this state, as shown in Fig. 1A, a solution 150 exists on a side surface of the amorphous silicon film 103. In this example, reference numeral 100 denotes a glass substrate, and 102 is a silicon oxide film which denotes an under layer.

With a heat treatment in this state, the nickel elements are diffused so that crystal growth proceeds in a direction parallel to the substrate as indicated by reference numeral 107 (207 in case of Fig. 2) (Figs. 1A and 2D).

In this crystal growth, since nothing is formed on the surface of the silicon film (at least an artificial film formation or processing is not conducted), crystal growth proceeds smoothly.

It is preferable that a temperature at which the above-described heat treatment is conducted for crystallization is selected from a range of 550 to 650 °C.

This is because when the temperature is lower than 550 °C, crystallization does

not proceed, whereas when the temperature is higher than 650 °C, crystallization not caused by the action of nickel proceeds to impede the crystallization caused by the action of nickel.

A configuration as indicated by reference numeral 205 in Fig. 2B (dimensions such as a length, a depth and a width) obtained by removing a part of the amorphous silicon film is important in controlling the crystallinity of the silicon film and the amount of metal elements.

Also, in a process shown in Figs. 2A to 2D, it is important to prevent the amorphous silicon film 203 from being oxidized and prevent another film from being laminated on the amorphous silicon film 203 prior to the processes shown in Figs. 1A and 2B.

As shown in Fig. 1B, in the case where the amorphous silicon film 103 is oxidized to form the silicon oxide film 104, because a sufficient water repellency (hydrophobic property) is not obtained by the silicon oxide film, the solution remains on the upper surface of the amorphous silicon film, thereby making it difficult to hold the metal elements in only the metal element added region.

Further, in the case where the crystallizing process which is a subsequent process is conducted, as shown in Fig. 1B, crystallization is impeded by an influence of an interface between the oxide film and the amorphous silicon film, thereby being not capable of obtaining an excellent crystallinity.

Also, as shown in Fig. 1C, crystal growth proceeds from an unintended region on the amorphous surface, to thereby come to a state where crystal growth proceeding from a specified region toward a direction parallel to the substrate is impeded, because, when crystal growth collides with crystal growth proceeding from a different region, grain boundaries are formed there to stop crystal growth.

For the above reasons, it is desirable that stains on the surface of the amorphous silicon film and a natural oxide film are removed by a hydrofluoric acid processing or the like before coating the solution containing the metal elements therein on the amorphous silicon film to thereby form a silicon film surface having a sufficient water repellency.

Also, it is preferable that the solution is coated on the amorphous silicon film without allowing the amorphous silicon film to be in contact with an oxidizing

atmosphere (for example, air) after the stains on the surface of the amorphous silicon film and the natural oxide film are removed by the hydrofluoric acid processing, etc., and then a heat treatment is conducted.

First Embodiment

Figs. 2A to 4K show a process of manufacturing a thin film transistor according to a first embodiment.

First, a silicon oxide film is formed in thickness of 30 nmÅ as an under film 202 on a quartz substrate 200. If the smoothness of the surface of the silica substrate is excellent, and the surface is sufficiently cleaned, the under film 202 is not particularly required.

Also, although the quartz substrate is used as an insulating substrate, a glass substrate, a single crystal silicon substrate or a polycrystal silicon substrate on a surface of which an insulating film is formed may be employed instead of the quartz substrate.

Subsequently, an amorphous silicon film 203 that serves as a starting film of the crystalline silicon film is formed in a thickness of 60 nm through the low pressure CVD method (Fig. 2A).

It is preferable that the thickness of the amorphous silicon film is set to 200 nm or less.

Then, an opening indicated by reference numeral 205 is defined on the amorphous silicon film. The opening 205 has a slender rectangular which is longitudinal along a backward direction and a forward direction of the figure. The width of the opening 205 is properly set to be 10 μm or more. Also, an end portion of the opening 205 is designed so as to be apart from an island region of an active layer which will be formed in a later process.

In the opening, the silicon oxide film 202 which is an under film is exposed.

Then, the stains on the surface of the amorphous silicon film and a natural oxide film are removed by a hydrofluoric acid processing or the like.

Thereafter, a nickel acetate solution containing nickel elements of 10 ppm in weight conversion therein is coated on the surface. Then, spin dry is conducted

using a spinner (not shown) to remove an excessive solution existing on the upper surface of the amorphous silicon film.

The nickel acetate solution has a sufficient water repellency to the amorphous silicon film. In this way, there is obtained a state in which the nickel elements exist in a state indicated by a dotted line 206 in Fig. 2C.

In this state, the nickel acetate solution is repelled by the surface of the amorphous silicon film in a region other than the opening 205. Then, there is obtained a state in which the nickel elements are selectively held in contact with a part of the amorphous silicon film on a side wall of the opening 205.

Thereafter, a heat treatment is conducted at 600°C for 8 hours in a nitrogen atmosphere containing 3% of hydrogen but oxygen as little as possible. With this process, as indicated by reference numeral 207 in Fig. 2D, crystal growth proceeds in a direction parallel to the substrate 200.

The crystal growth proceeds from the region of the opening 205 into which the nickel elements are introduced (a metal element added opening) toward a direction parallel to the substrate.

The surface of the crystalline silicon film that has laterally grown as obtained by this crystal growth is very excellent in smoothness in comparison with the conventional low-temperature polysilicon or high-temperature polysilicon. It is presumed that this is because directions along which grain boundaries extend are roughly uniform.

The silicon film which is called generally polycrystal silicon or polysilicon has a surface roughness of ±10 nm or more. However, in the case of allowing lateral growth as described in this embodiment, it is observed that the surface roughness is ±3 nm or less. The roughness deteriorates the characteristics of the interface between the silicon film and the gate insulating film, and therefore the roughness is preferably made as small as possible.

In the heat treatment condition for the above-described crystallization, the lateral growth can be conducted over 100 μm or more.

After the state shown in Fig. 2D is obtained, a laser light may be irradiated thereonto. In other words, the crystallization may be further promoted by the irradiation of a laser light. The irradiation of the laser light has the effect of diffusing a

mass of nickel elements existing in the film so that the nickel elements are liable to be removed later. Even if the laser light is irradiated thereon at this stage, the lateral growth does not further proceed.

The laser light to be used may be an excimer laser having the wavelengths of an ultraviolet region. For example, KrF excimer laser (248 nm in wavelength) or XeCl excimer laser (308 nm in wavelength) can be employed.

Thereafter, a heat treatment is conducted at 950 °C in an oxygen atmosphere containing halogen elements, for example, an oxygen atmosphere containing HCl of 3 vol% therein, to form a thermal oxide film in a thickness of 200 Å (not shown). The thickness of the silicon film is reduced about 100 Å according to the formation of the thermal oxide film. That is, the thickness of the silicon film is set to be about 500 Å.

In this process, the silicon elements having an unstable bonding state in the film are utilized for the formation of the thermal oxide film when the thermal oxide film is formed. Then, defects in the film are reduced, thereby being capable of obtaining higher crystallinity.

Also, the gettering of the nickel elements in the film is conducted due to the formation of the thermal oxide film and the action of chlorine.

After the formation of the thermal oxide film, the thermal oxide film (not shown) is removed. In this way, a crystalline silicon film in which the content concentration of the nickel elements is reduced, is obtained. The crystalline silicon film thus obtained has a structure in which crystal structures extend in one direction (this direction is identical with the crystal growth direction). That is, the crystalline silicon film has a structure in which a plurality of slender columnar crystals are aligned in parallel through a plurality of grain boundaries that extend in one direction.

Thereafter, patterning is conducted to form a pattern of a lateral growth region. An island region 301 of this region will form an active layer of a TFT later (Fig. 3E).

In this process, the island region 301 is positioned in such a manner that a direction connecting a source region and a drain region is identical or substantially identical with the crystal growth direction. This enables a direction along which carriers move to be identical with a direction along which crystal lattices continuously extend, with the result that a TFT having a high-characteristic can be obtained.

Then, after the formation of the island region 301, a silicon oxide film 315 is formed in a thickness of 500 Å through the plasma CVD method (Fig. 3F).

Furthermore, a thermal oxide film 311 is formed in a thickness of 300 Å through the thermal oxidation method. In this way, a gate insulating film 800 Å in thickness which is formed of a CVD silicon oxide film 315 and the thermal oxide film 311 is obtained (Fig. 3G).

With the formation of the gate insulating film, the thickness of the island region 301 that will form the active layer becomes 350 Å. This is because the formation of the thermal oxide film 311 having a thickness of 300 Å makes the surface of the island region 301 reduce to the thickness of 150 Å.

Thereafter, an aluminum film for forming a gate electrode is formed in a thickness of 4,000 Å through the sputtering method. 0.2 wt% of scandium is allowed to be contained in the aluminum film.

The reason why scandium is allowed to be contained in the aluminum film is to suppress hillock or whisker from occurring in a later process. The hillock or whisker is directed to a needle-shaped or sharp projection caused by abnormal growth of aluminum at the time of heating.

A material for forming the gate electrode may be tantalum (Ta), polycrystal silicon doped with phosphorus (P) with a high concentration, silicide of tungsten (WSi), or a structure in which polycrystal silicon doped with phosphorus and silicide of tungsten are laminated or hybridized, other than aluminum.

After the formation of the aluminum film, a dense anodic oxide film (not shown) is formed. The anodic oxide film is formed under the condition where an electrolyte is an ethylene glycol solution containing 3% of tartaric acid, an anode is formed of an aluminum film and a cathode is made of platinum. In this process, the anodic oxide film having a dense film quality is formed in a thickness of 100 Å on the aluminum film.

The anodic oxide film not shown serves to improve the adhesion to a resist mask 322 which will be formed later.

The thickness of the anodic oxide film can be controlled by applied voltage at the time of anodic oxidation.

Then, a resist mask is formed. Using this resist mask, the aluminum film is

patterned to a pattern 318. Thus, a state shown in Fig. 3H is obtained.

In this situation, anodic oxidation is again conducted. In this process, a 3% of oxalic acid aqueous solution is used as the electrolyte. In this electrolyte solution, anodic oxidation is conducted with the pattern 318 of aluminum as an anode, to thereby form a porous anodic oxide film.

In this process, porous anodic oxide films 419 are selectively formed on a side surface of the aluminum pattern because a high-adhesive resist mask 322 exists on the upper portion. (Fig. 4)

The porous anodic oxide films 419 can be allowed to grow up to the thickness of several μm. In this embodiment, the thickness is set to be 6,000 Å. The growth distance can be controlled according to an anodic oxidation time.

Then, the resist mask 322 is removed. Subsequently, a dense anodic oxide film 420 is again formed. In other words, anodic oxidation is again conducted with the above-mentioned ethylene glycol solution containing 3% of tartaric acid as the electrolyte.

In this process, a dense-quality anodic oxide film is formed as indicated by reference numeral 420 because the electrolyte enters the porous anodic oxide films 419.

The thickness of the dense anodic oxide film 420 is set to be 1,000 Å. The thickness is controlled by applied voltage.

In this situation, the exposed silicon oxide film 315 is etched. Also, the gate insulating film formed of the CVD silicon oxide film 315 and the thermal oxide film 311 is etched. The etching is made by dry etching.

In this way, a state shown in Fig. 4J is obtained. Then, using a mixture acid in which acetic acid, nitric acid and phosphoric acid are mixed together, the porous anodic oxide films 419 are removed.

After the state shown in Fig. 4J is obtained, impurity ions are implanted. In this embodiment, in order to manufacture an n-channel thin film transistor, P (phosphorus) ions are implanted through the plasma doping method.

In this process, regions 430 and 434 to be heavy-doped and regions 431 and 433 to be light-doped are formed. This is because the remaining silicon oxide film 315 functions as a translucent mask to shield a part of ions as implanted there.

Then, a laser light (or an intense light using a lamp) is irradiated to activate the region into which the impurity ions are implanted. Thus, a source region 430, a channel forming region 432, a drain region 434, and low-concentration impurity regions 431 and 433 are formed in a self-alignment manner.

In this embodiment, what is indicated by reference numeral 433 is a region called "LDD (light dope drain) region". (Fig. 4J)

In the case where the thickness of the dense anodic oxide film 420 is set to 2,000 Å or more, offset gate regions can be formed outside of the channel forming region 432 with that thickness.

In this embodiment, the offset gate regions are formed, but since their dimensions are small, the contribution of the offset gate regions is small, and in order to avoid complexity of the drawings, the offset gate regions are not shown in the figures.

Thereafter, a silicon oxide film, a silicon nitride film or a laminated film of those films is formed as an interlayer insulating film 440. The interlayer insulating film may be a layer made of a resin material formed on a silicon oxide film or a silicon nitride film.

Then, contact holes are formed to form a source electrode 441 and a drain electrode 442. In this way, a thin film transistor shown in Fig. 4K is completed.

Second Embodiment

A second embodiment is directed to an example in which a hydrophobic property of the surface of an amorphous silicon film is selectively controlled so as to selectively manufacture TFTs different in crystallinity.

In other words, there is shown an example in which an oxide film is formed on a part of the amorphous silicon film to improve the wettability of that region (that is, the hydrophobic property is reduced), and a large amount of nickel elements are selectively introduced in only the region.

In general, in the case where the concentration of metal elements is increased, high crystallinity is obtained, and the movability of the TFT as obtained becomes large. However, the characteristic instability and an off-state current value become

large.

Also, as a general theory, a p-channel TFT (PTFT) is stable in characteristic but small in movability. On the other hand, an n-channel TFT (NTFT) has an tendency that it is large in movability but unstable in characteristic because of the hot carrier effect.

Under the above circumstances, in this embodiment, the crystalline silicon film that forms a p-channel TFT is manufactured using metal elements with a high concentration, whereas a crystalline silicon film that forms an n-channel TFT is manufactured using metal elements with a low concentration.

Figs. 6A to 6F show a manufacturing process according to the second embodiment. First, a silicon oxide film 602 is formed as an under film on a glass substrate 601 (or quartz substrate).

Then, an amorphous silicon film 603 is formed through the low pressure CVD method.

Thereafter, an extremely thin oxide film (not shown) is selectively formed on the entire surface, and an oxide film 604 is also selectively formed thereon. In this example, an oxide film is formed by the irradiation of UV rays in an oxidization atmosphere. The method of forming the oxide film may be a method of using an oxidation acting solution such as ozone water.

In this way, a state shown in Fig. 6A is obtained. Then, a nickel acetate solution is coated on the surface. In this process, only a region where the oxide film 604 is formed is held in contact with nickel elements because the surface of the oxide film 604 is deteriorated in hydrophobic property (Fig. 6B).

On the other hand, since the nickel acetate solution is repelled by the surface of the amorphous silicon film, the nickel elements are not introduced into a region where the oxide film 604 is not formed.

Then, a heat treatment is conducted. The heat treatment is conducted at 600 °C for 4 hours in a nitrogen atmosphere.

The entire of the amorphous silicon film is crystallized in this heat treatment. In this process, first, in the region where the oxide film 604 is formed, that is, the region where the nickel elements are introduced (the nickel addition region), crystals grow vertically. On the other hand, in the region where the oxide film 604 is not formed,

that is, the region where the nickel elements are not introduced (the no nickel addition region), crystals grow laterally from the nickel addition region. However, in the no nickel addition region, natural nucleation also occurs before the crystal lateral growth starts. As a result, crystals by the lateral growth and the natural nucleation are mixed in the no nickel addition region, so that the crystallinity in the nickel no addition region becomes lower than that in the nickel addition region.

Because the nickel elements exist in the nickel addition region, the crystal nucleation can be controlled. But, in the no nickel addition region, natural nucleation which cannot be controlled also occurs. Therefore, it results in the no nickel addition region having a lower crystallinity than the nickel addition region.

Thus, a region 606 higher in crystallinity and a region 607 lower in crystallinity are obtained (Fig. 6C).

Subsequently, patterning is conducted to form regions 608 and 609. In this situation, the crystallinity of the region 608 is higher than that of the region 609. Those regions will form active layers of a TFT later (Fig. 6D).

Thereafter, a gate insulating film 600 is formed. Then, gate electrodes 610 and 612 made of aluminum are formed. Anodic oxide films 611 and 613 are formed in the periphery of the gate electrode.

Then, doping with phosphorus and born is selectively conducted, to thereby form a source region 614, a channel forming region 615 and a drain region 616 of a PTFT in a self-alignment manner (Fig. 6E).

Simultaneously, a source region 617, a channel forming region 618 and a drain region 619 of an NTFT are formed in a self-alignment manner (Fig. 6E).

Subsequently, an interlayer insulating film 620 is formed, and contact holes are also defined to form a source electrode 621 and a drain electrode 622 of the PTFT. Also, a source electrode 623 and a drain electrode 624 of the NTFT are formed.

In this way, the PTFT and the NTFT are obtained. In this structure, the crystallinity of the active layer that forms the PTFT is higher than that of the active layer that forms the NTFT.

Accordingly, the movability of the PTFT can be relatively increased. Since the characteristics of the PTFT are more stable than those of the NTFT, even if the concentration of nickel elements becomes slightly high, there arises no problem on

the whole.

On the other hand, in the NTFT, the concentration of nickel elements in the active layer is reduced so as to enhance the stability of the characteristics.

In this way, a difference in movability between the PTFT and the NTFT can be corrected so that a difference in stability therebetween can be further corrected.

As is described above, according to the present invention, using the hydrophobic property of the silicon film, when the solution containing the metal elements that promote the crystallization of silicon therein is coated, selective coating is realized, thereby being capable of conducting crystal growth in a direction parallel to the substrate. In this structure, since no mask that impedes crystal growth is formed on the upper portion of the crystal growth region, the crystal growth is not impeded, thereby being capable of obtaining the crystalline region high in quality.

Using this technique, a TFT having a high characteristic can be obtained with a high productivity and uniform characteristic.

The present invention described in this specification is applicable to not only the structure of a peripheral circuit formed together with an active matrix circuit on the same substrate in a transparent or reflection type active matrix liquid-crystal display device, but also a display device having an EL (electro luminescence) element, and a variety of circuits using a thin film transistor.

Also, the present invention described in this specification is applicable to the manufacture of a variety of integrated circuits using a thin film transistor and a device using those various integrated circuits. The device of this type may be, for example, a portable information processing terminal or a video camera.

WHAT IS CLAIMED IS:

1. A method of manufacturing an EL display device, said method comprising the steps of:

forming an amorphous semiconductor film comprising Si_XGe_{1-X} ($0<x<1$) on an insulating surface;

removing a portion of the amorphous semiconductor film to form a metal element addition region, where a metal element is capable of promoting crystallization of the amorphous semiconductor film;

selectively introducing the metal element in contact with the metal element addition region;

heating the amorphous semiconductor film so that crystals grow in parallel to the insulating surface from the metal element addition region,

wherein the selectively introducing the metal element is selectively comprises coating a solution containing the metal element therein and applying water repellence of the semiconductor film to the solution.

2. A method according to claim 1,

wherein a surface of a region where crystal growth is conducted is exposed in crystal growth.

3. A method according to claim 1,

wherein the metal element is at least one selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

4. A method of manufacturing an EL display device, said method comprising steps of:

forming an amorphous semiconductor film comprising Si_XGe_{1-X} ($0<x<1$) on an insulating surface;

removing a portion of the semiconductor film to form a metal element addition region, where a metal element is capable of promoting crystallization of the amorphous semiconductor film;

introducing the metal element in contact with the metal element addition region;

heating the amorphous semiconductor film so that crystals grow in parallel to the insulating surface from the metal element region;

forming a semiconductor island using the crystallized semiconductor film;

forming a gate electrode adjacent to the semiconductor island having a gate insulating film therebetween;

introducing an impurity into the semiconductor island to form at least a source region, a drain region, and a channel region between the source and drain regions,

wherein the metal element is selectively introduced by coating a solution containing the metal element therein and applying water repellency of the semiconductor film to the solution.

5. A method according to claim 4,

wherein the metal element is one selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

6. A method of manufacturing an EL display device, said method comprising the steps of:

forming an amorphous semiconductor film comprising Si_XGe_{1-X} ($0<x<1$) on an insulating surface;

removing a portion of the semiconductor film to form a metal element addition region, where a metal element is capable of promoting crystallization of the amorphous semiconductor film;

introducing the metal element in direct contact with the metal element addition region; and

crystallizing the amorphous semiconductor film in a parallel direction to the insulating surface from the metal addition region by heating;

forming a semiconductor island using the crystallized semiconductor film;

forming a gate electrode adjacent to the semiconductor island having a gate insulating film therebetween;

introducing an impurity into the semiconductor island to form at least a source region, a drain region, and a channel region between the source and drain regions;

forming an insulating film covering the semiconductor island and the gate electrode;

forming at least an electrode being connected to at least one of the source and drain regions through the insulating film,

wherein the metal element is selectively introduced by coating a solution containing the metal element therein and applying water repellency of the semiconductor film to the solution.

7. A method according to claim 6,

wherein the metal element is at least one selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

ABSTRACT

A method of manufacturing a crystalline silicon film excellent in crystallinity. When using elements such as nickel as metal elements that promotes the crystallization of the amorphous silicon film, nickel is allowed to be contained in a solution repelled by the surface of the amorphous silicon film. Then, a part of the amorphous silicon film is removed, and the solution is held in only that part. In this way, the nickel elements are selectively introduced into a part of the amorphous silicon film, and a heat treatment is also conducted to allow crystal growth to proceed from that portion toward a direction parallel to a substrate.

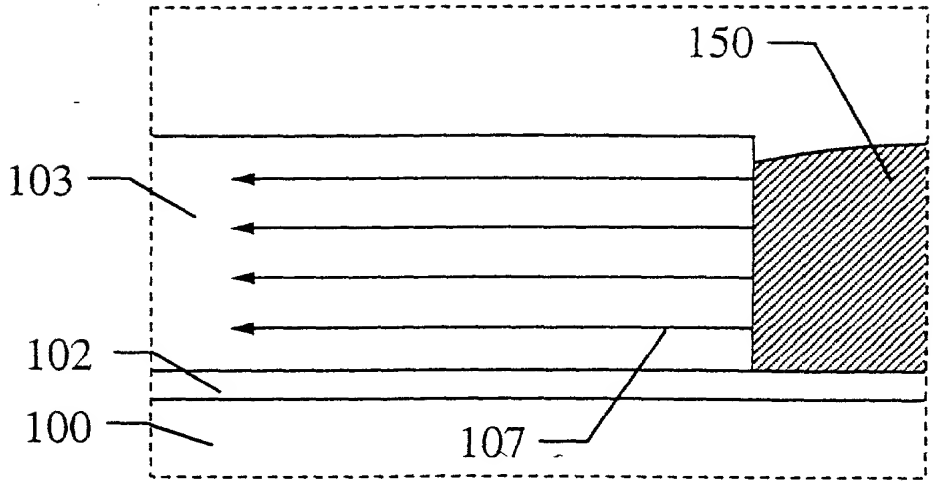

FIG. 1A

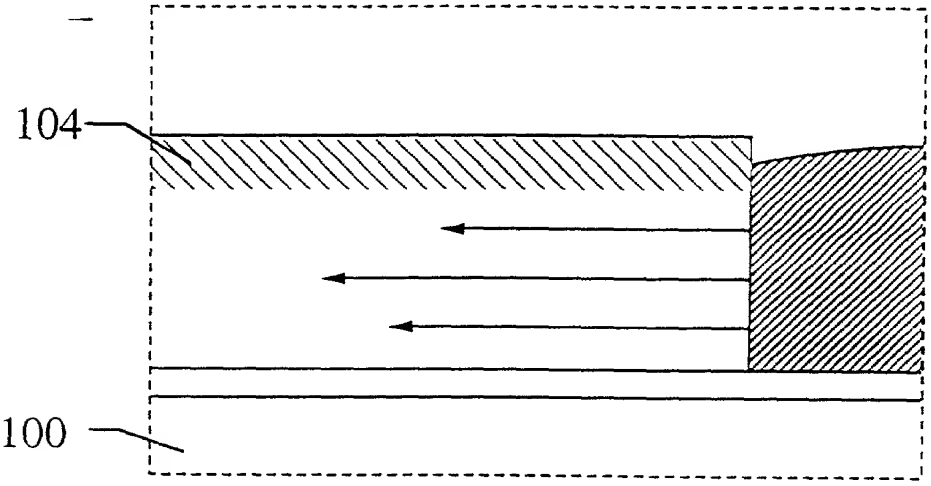

FIG. 1B

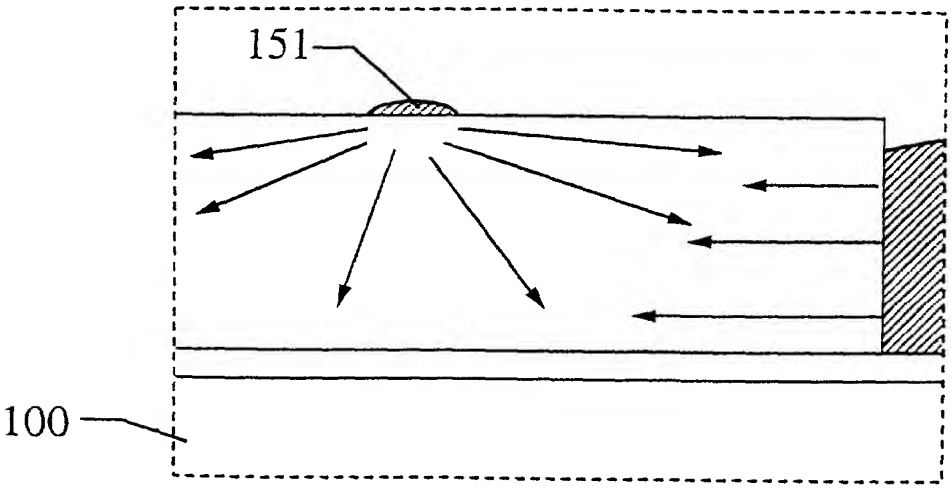

FIG. 1C

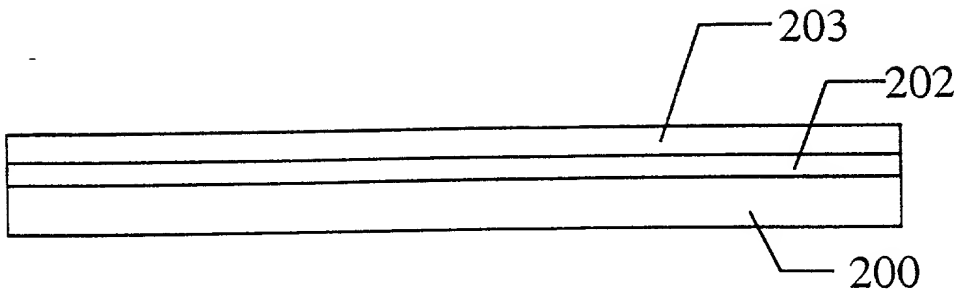

FIG. 2A

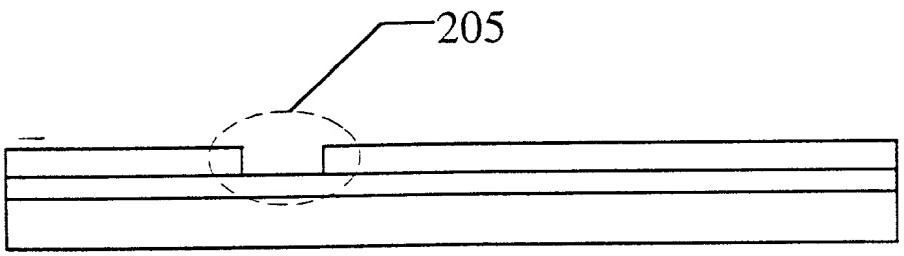

FIG.2B

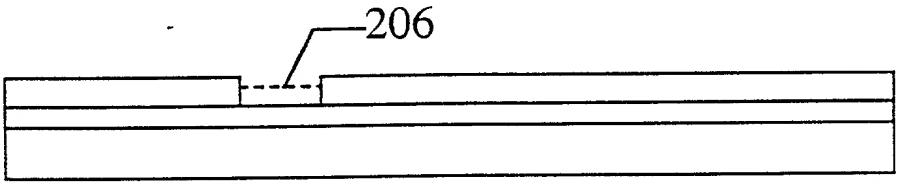

FIG. 2C

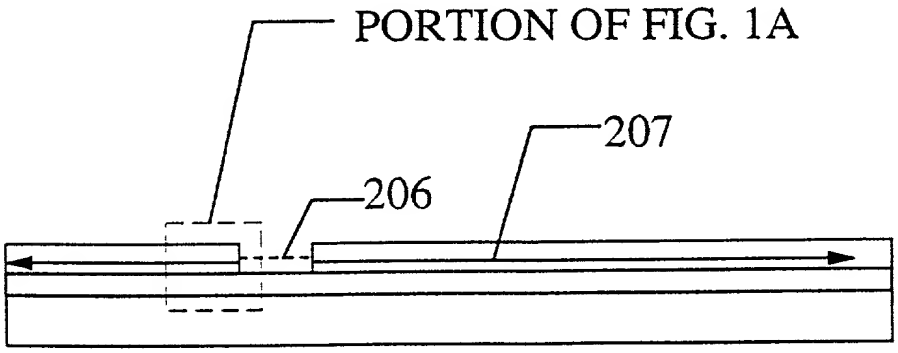

FIG. 2D

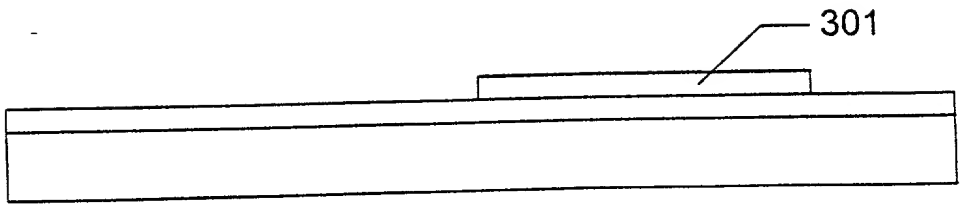

FIG. 3E

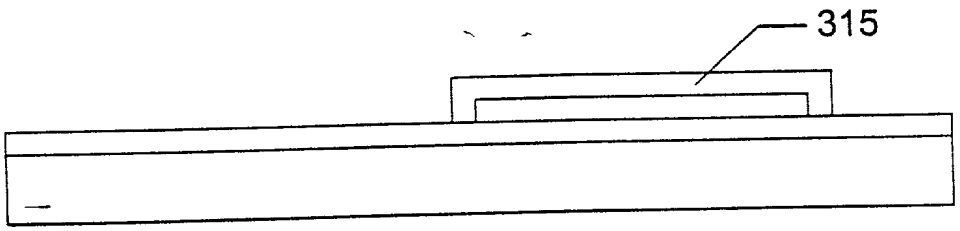

FIG. 3F

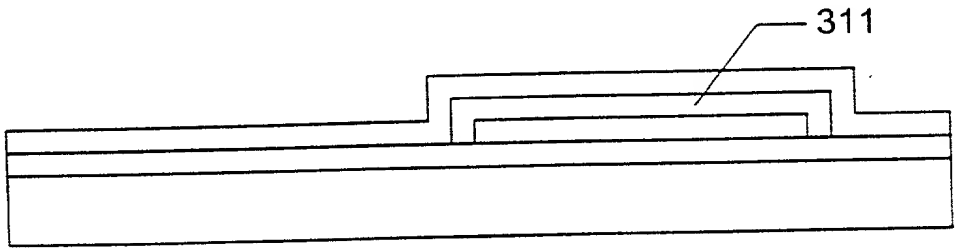

FIG. 3G

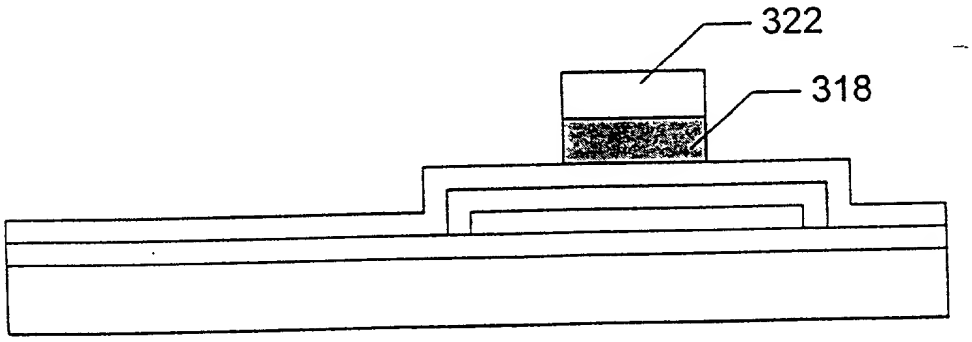

FIG. 3H

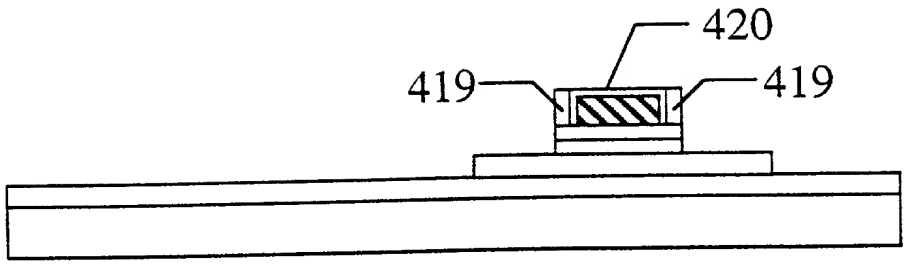

FIG. 4I

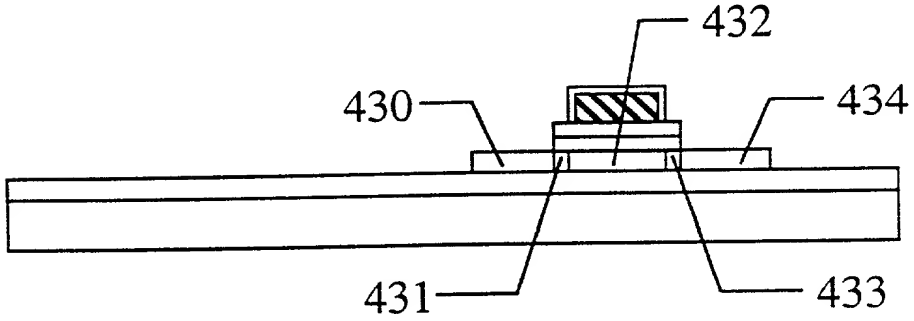

FIG. 4J

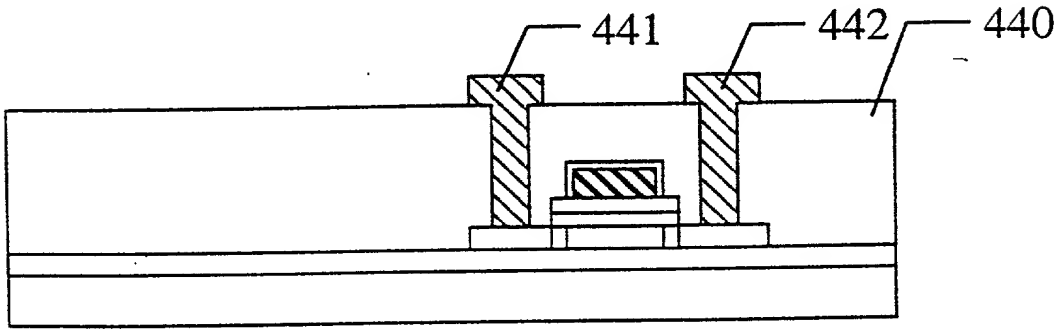

FIG. 4K

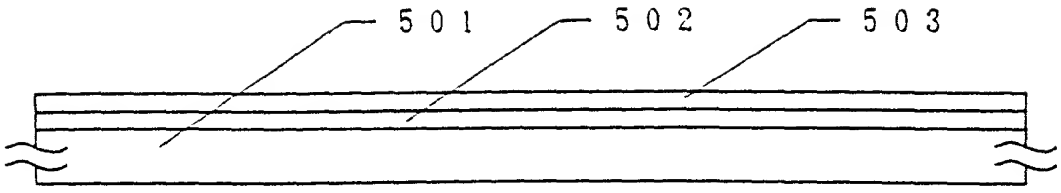

FIG. 5A PRIOR ART

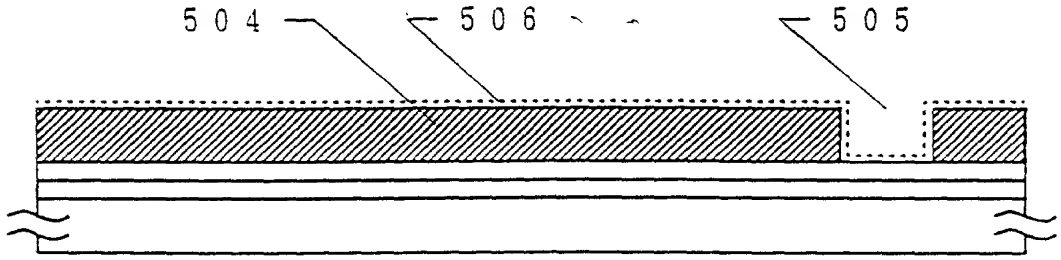

FIG. 5B PRIOR ART

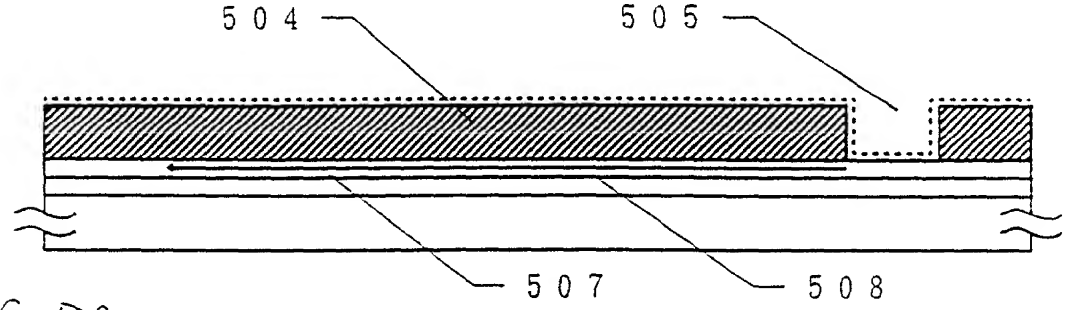

FIG. 5C PRIOR ART

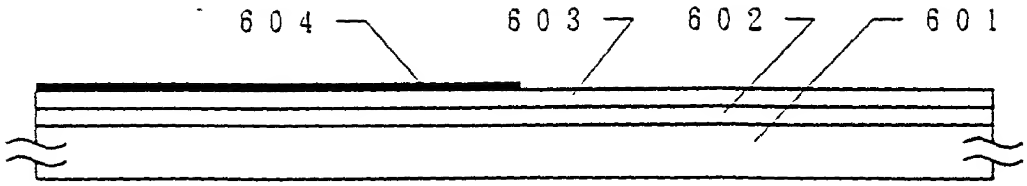

FIG. 6A

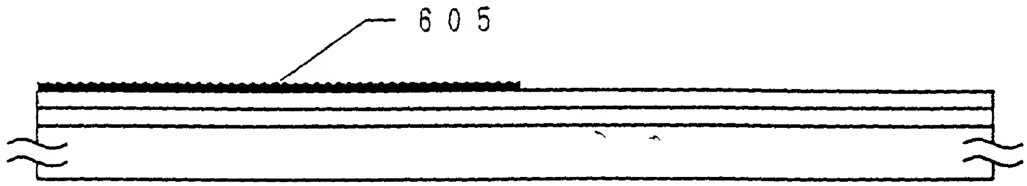

FIG. 6B

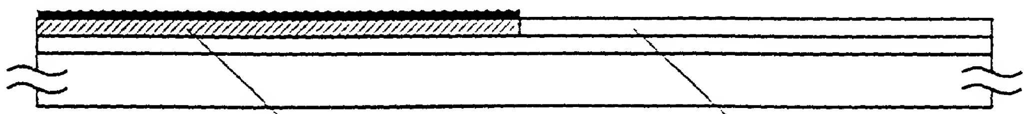

FIG. 6C

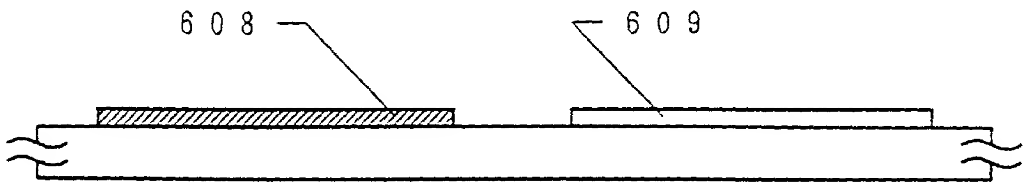

FIG. 6D

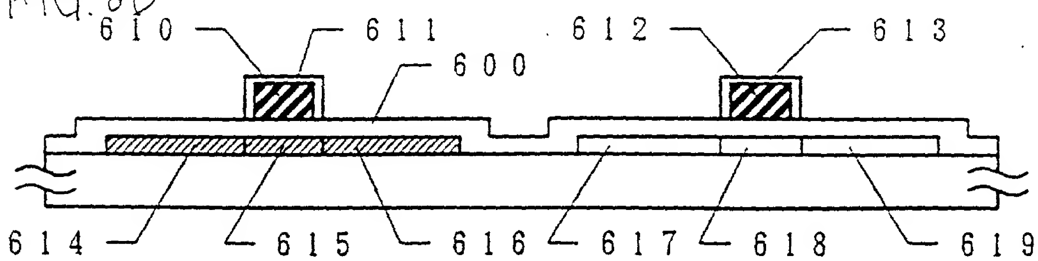

FIG. 6E

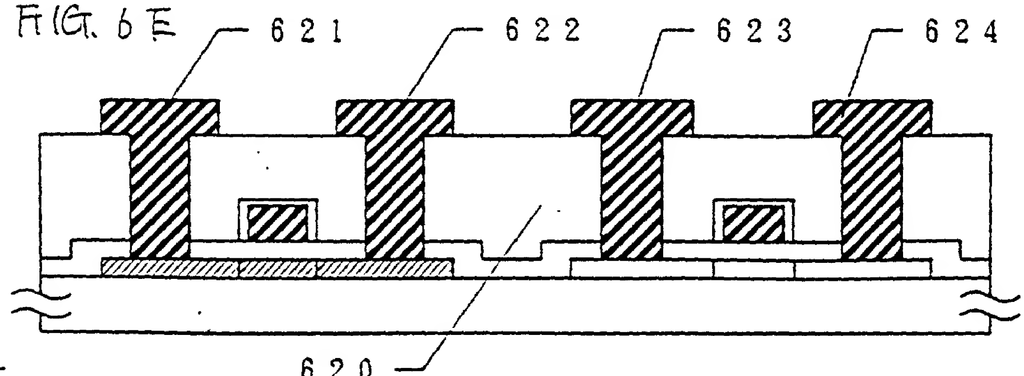

FIG. 6F

PTO/SB/105 (8-96)
Approved for use through 9/30/98 OMB 0651-0032
Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

上記発明の明細書（下記の欄でXBがついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ ＿月＿日に提出され、米国出願番号または特許協定条約国際出願番号を＿＿＿＿＿＿とし、
（該当する場合）＿＿＿＿＿＿ に訂正されました。

☐ was filed on ＿＿＿＿＿＿
as United States Application Number or
PCT International Application Number
＿＿＿＿＿＿ and was amended on
＿＿＿＿＿＿ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

PTO/SB/106 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条(a)-(d)又は３６５条(b)に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約３６５(a)に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、各欄をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed 優先権主張なし
9-53843 (Number) (番号)	Japan (Country) (国名)	February 20, 1997 (Day/Month/Year Filed) (出願年月日)	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐

私は、第３５編米国法典１１９条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(c)に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際出願日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は発行された特許の有効性が失われることを認識し、よってここに下記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

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Scott C. Harris
(619) 678-5070

唯一または第一発明者		Full name of sole or first inventor Hisashi OHTANI	
発明者の署名	日付	Inventor's signature Hisashi Ohtani	Date February 4, 1998
住所		Residence Kanagawa, Japan	
国籍		Citizenship Japanese	
私書箱		Post Office Address c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan	
第二共同発明者		Full name of second joint inventor, if any	
発明者の署名	日付	Inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	

(第三以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for third and subsequent joint inventors.)

☐ Please see attached page 3a for names, addresses and signatures of additional inventors, if any.